## CLAIMS

What is claimed is:

1. A method for dynamically correcting an aspect of an electromagnetic wave being processed, said method comprising the steps of:

processing two or more aspects of said electromagnetic wave along two or more separate signal paths;

comparing an expected value for at least one of said aspects of said electromagnetic wave along at least one of said signal paths with an actual value for said aspect of said electromagnetic wave along said at least one signal path to generate a correction signal; and

applying said correction signal to at least one other aspect of said electromagnetic wave.

2. A method as in claim 1, wherein said two or more aspects of said electromagnetic wave comprise amplitude and phase information for said electromagnetic wave.

3. A method as in claim 1, wherein said aspect of said electromagnetic wave that is compared is phase information for said electromagnetic wave.

4. A method as in claim 1, wherein said step of applying said correction signal to said other aspect of said electromagnetic wave is accomplished by compensating for an analog delay.

5. A method as in claim 1, wherein said actual value is digitized into a digital signal using a quantizer.

6. A method as in claim 1, wherein said step of comparing said expected value to said actual value is accomplished using a digital phase-locked loop.

7. A method as in claim 4, wherein said step of applying said correction signal to said other aspect of said electromagnetic wave is accomplished using a bank of pipeline registers.

8. A method as in claim 1, wherein said step of applying said correction signal to said other aspect of said electromagnetic wave is accomplished by compensating for a digital delay.

9. A method as in claim 1, wherein said step of applying said correction signal to said other aspect of said electromagnetic wave is accomplished by determining a digital delay between at least two of said aspects of said electromagnetic wave using a difference in clock periods between at least two of said aspect signals.

10. A method for dynamically correcting a signal being processed, said method comprising the steps of:

processing an amplitude aspect and a phase aspect of said signal along an amplitude and a phase paths, respectively;

quantizing said phase aspect of said signal to generate an actual phase value;

comparing said actual phase value with an expected phase value to determine any delay in an analog portion of said phase path in relation to said amplitude path;

generating a correction signal based upon said comparison; and

using said correction signal to adjust said amplitude aspect of said signal.

11. The method of claim 10, wherein said comparison of said expected value to said actual value is accomplished using a digital phase-locked loop.

12. The method of claim 10, wherein said adjustment of said amplitude aspect of said signal is accomplished using a bank of pipeline registers.

13. The method of claim 10, further comprising the steps of:

determining any delay in a digital portion of said phase path using a difference in clock periods between said amplitude and phase aspects of said signal along said paths;

generating another correction signal; and

using said another correction signal to adjust said amplitude aspect of said signal.

14. The method of claim 13, wherein said adjustment of said amplitude aspect of said signal is accomplished using at least one pipeline register.

15. An apparatus for dynamically correcting a signal comprising:

at least one signal path for processing at least one aspect of said signal;

at least one separate signal path for processing at least one other aspect of said signal;

a correction circuit for generating a digital value of said one aspect along said one signal path, comparing said digital value with an expected value to determine any delay in an analog portion of said signal path relative to said separate signal path, generating a correction signal based upon said comparison, and using said correction signal to adjust said other aspect of said signal.

16. The apparatus of claim 15, wherein said aspects of said signal comprise amplitude and phase information.

17. The apparatus of claim 15, wherein said aspect of said signal that is compared is phase information.

18. The apparatus of claim 15, wherein said comparison circuit comprises a quantizer for generating said digital value of said one aspect.

19. The apparatus of claim 15, wherein said comparison circuit comprises a digital phase-locked loop for comparing said digital value with said expected value.

20. The apparatus of claim 15, wherein said comparison circuit comprises a bank of pipeline registers for adjusting said other aspect of said signal.

21. The apparatus of claim 15, wherein said comparison circuit further comprises a processor for determining any delay in a digital portion of said one path relative to said separate path using a difference in clock periods between said aspects of said signal along said paths, generating another correction signal, and using said another correction signal to adjust said other aspect of said signal.

22. The apparatus of claim 21, wherein said processor comprises at least one pipeline register.

23. An apparatus for dynamically correcting a signal comprising:

at least one signal path for processing the phase of said signal;

at least one separate signal path for processing the amplitude of said signal;

a quantizer for generating a value of said phase along said one signal path;

a digital phase locked loop for comparing said value with an expected value to determine any delay in an analog portion of said one signal path relative to said separate signal path, and to generate a correction signal based upon said comparison; and

a bank of pipeline registers for adjusting said separate signal path.

24. The apparatus of claim 23, further comprising a processor for determining any delay in a digital portion of said one path relative to said separate path using a difference in clock periods along said paths, generating another correction signal, and using said another correction signal to adjust said separate signal path.

25. The apparatus of claim 24, wherein said processor comprises at least one pipeline register.